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For additional information, visit

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings

Optical Transmitter

For additional information, visit

For additional information, visit

Optical Receiver

The 800G DR8/DR8+ optical transceiver electrical interface is based on (2x of) the IEEE 802.3ck 400GAUI-4 host to module retimed interface (per IEEE 802.3ck Annex 120G). The 800G DR8/DR8+ optical receiver is compliant with (2x of) the IEEE 802.3bs 400GBASE-DR4 standard on 8 channels of 100G PAM4 data on parallel single-mode fber (100G per fber), with additional optical reach of up to 2 km. Each optical lane is compliant with the IEEE 802.3cu 100G-FR1 optical interface specifcation. The DR4 and FR1 optical interface standards are defned assuming IEEE standard 400G KP4 RS(544,514) forward error correction (FEC) implemented in the host or switch equipment in order to enable error-free link operation.

100G/lane specifcations are shown below; the 800G DR8/DR8+ optical transceiver also supports a software /Dcl v ᵀ ɾ " ˢ

For additional information, visit

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Damage threshold		-	-	5	dBm	1
Average receive power		-5.9	-	4	dBm	
Receive power in OMA_{outer}		-	-	4.2	dBm	
Receiver reflectance		-	-	-26	dB	
Unstressed receiver sensitivity (OMA_{outer}	URS	max(-3.9, SECQ-5.3)			dBm	2
Stressed receiver sensitivity (OMA_{outer}	SRS	-	-	-1.9	dBm	
(SECQ)	SECQ	3.4			dB	3

(1) The receiver is able to tolerate, without damage, continuous exposure to a signal having this average optical power level.

Electrical PIN Assignment

For additional information, visit

PAD	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE	NOTES
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	

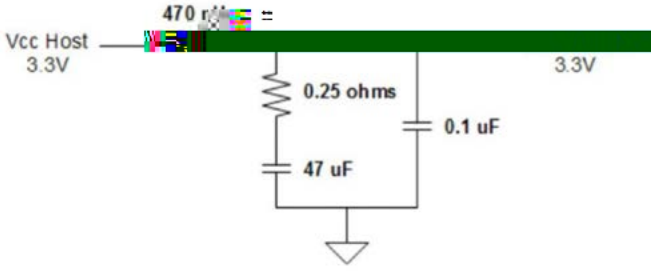
For additional information, visit

Power Supply

Here we describe the power supply filtering requirements and the power supply sequencing requirements.

The power supply filtering requirements for the 800G DR8/DR8+ OSFP Optical Transceiver have been designed to be consistent with those required for OSFP modules. A representative power supply filtering circuit for use on the host board is shown in the figure below.

One filtering circuit is recommended for each power supply rail.



Power supply specifications for the module are defined below. The module is compliant with OSFP Power Class 8.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
	VCC	3.135	3.3	3.465	V
		-	-	25	mV
		-	-	15	mV
	$PSNR_{mod}$	-	-	66	mV
	T_ip	-	-	50	µs
	T_init	-	-	500	ms
Inrush and discharge current	I_didt	-	-	100	mA/µs
High power to low power mode transition time (**)	T_hplp	-	-	200	µs

(*) Measured including ripple, droop, and noise below 100 kHz.

(**) From assertion of M_LPWn or M_RSTn or ForceLowPwr. I_didt will not be exceeded for any power transient events, including hot plug/unplug, power up/down, initialization, low-power to high-power and high-power to low-power transitions.

For additional information, visit

Control and Monitoring Interface

The optical transceiver supports a full CMIS-compliant set of control, alarm, and monitoring features through a standard I^2C management interface, as well as low speed control pins, which support additional module control and interrupt features.

In addition to the I^2C interface, the optical transceiver also supports low speed control pins, which provide immediate easy access to key module functions and provide additional user interface signals to support the management interface.

INT/RSTn is a dual-function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The host circuit enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host, which is translated to an active-low signal on the module. Interrupt is an active high signal on the module, which gets translated to an active low signal on the host.

The INT/RSTn signal operates in three voltage zones to indicate the state of reset for the module and interrupt for the host:

- Module in reset, interrupt deasserted (M_RSTn=Low, H_INTn=High). See table below for min/max voltages for Zone 1.
- Reset deasserted (M_RSTn=High) and interrupt deasserted (H_INTn=High). See table below for min/max voltages for Zone 2.
- Module out of reset and interrupt asserted (M_RSTn=High, H_INTn=Low). See table below for min/max voltages for Zone 3.

The table below shows voltage ranges for these three zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal, and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

PARAMETER	MIN	NOMINAL	MAX	UNITS	NOTE
Host VCC	3.135	3.300	3.465	Volts	VCC voltage on the host
H_Vref_INTn	2.475	2.500	2.525	Volts	Precision voltage reference for H_INTn
M_Vref_RSTn	1.238	1.250	1.263	Volts	Precision voltage reference for M_RSTn
	66k	68k			

LPWn/PRSn is a dual-function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The host circuit enables multilevel signaling to provide direct signal control in both directions. Low Power mode is an active low signal on the host, which gets converted to an active low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active low logic signal on the host.

The LPWn/PRSn signal operates in three voltage zones to indicate the state of Low Power mode for the module and Module Present for the host:

- Module present and in low power mode (M_LPWn=Low, H_PRSn=Low). See table below for min/max voltages for Zone 1.
- Module present and in high power mode (M_LPWn=High, H_PRSn=Low). See table below for min/max voltages for Zone 2.
- Module not present (H_PRSn=High). See table below for min/max voltages for Zone 3.

The table below shows voltage ranges for these three zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the host will assert Low Power mode on the module (M_LPWn=Low), at which point the module will transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp.

The LPWn/PRSn signal is driven high or open by the host for Low Power mode control. If logic is used to generate the high level, then 3.3V LVCMOS is preferred.

The module transmitters are disabled when in low power mode. In addition, a software-controlled transmitter disable is provided by the TX Disable register via the I2C interface.

The SCL pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface clock for the module. The SCL signal requires a pull-up resistor on the host board, between 1 kΩ and 4.7 kΩ depending on capacitive load. Note that SCL and SDA timing specifications are defined in section “Management Interface Timing.”

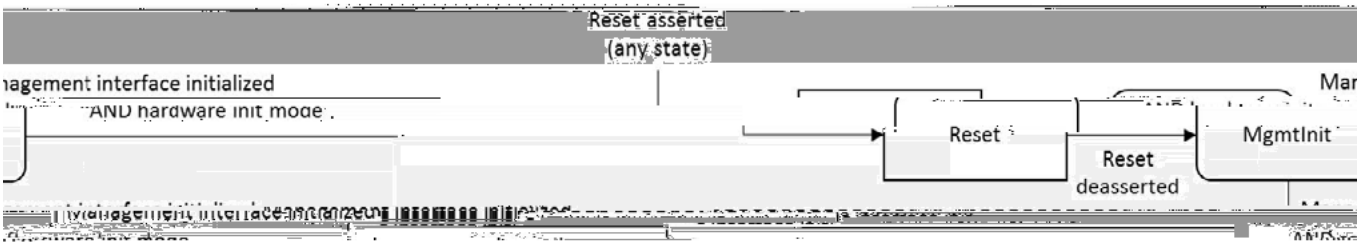
The SDA pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface data for the module. The SDA signal requires a pull-up resistor on the host board, between 1 kΩ and 4.7 kΩ depending on capacitive load. Note that SCL and SDA timing specifications are defined in section “Management Interface Timing.”

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
SCL and SDA	VOL	0	0.4	V	IOL_{max} = 3 mA
	VOH	Vcc-0.5	Vcc+0.3		
	VIL	-0.3	Vcc*0.3		
	VIH	Vcc*0.7	Vcc+0.5		
Capacitance					

Management Interface

An I2C interface shall be used for management interface between the optical transceiver and the host system. The communication protocol shall follow the industry standard Common Management Interface Specification (CMIS). Additional detail and clarified functionality are described in this sub-section.

The module behavior during power-up, mode changes, and fault conditions complies with the Common Management Interface Specification (CMIS), as outlined in the state machine diagrams and descriptions below.



STATE	POWER MODE	EXIT CONDITION	INTERRUPT CLASS	DATA PATH STATE
Reset	Low power	Reset signal deasserted	Suppress all	DeLE

STATE	TX OUTPUT STATE	RX OUTPUT STATE	INTERRUPT CLASS	EXIT CONDITION
DataPathDeactivated	Quiescent	Quiescent	Suppress all data path flags	Host sets DataPathPwrUp bit(s)
DataPathInit	Quiescent	Quiescent	Suppress all	Module completes data path power up and initialization
DataPathActivated	See Byte 54h	Active	All data path flags permitted	1) Host cle 6.1 (iTq ())1.118 0 Txd04l.8 (t) Hnpae2.t0i Quiescent Quiesc

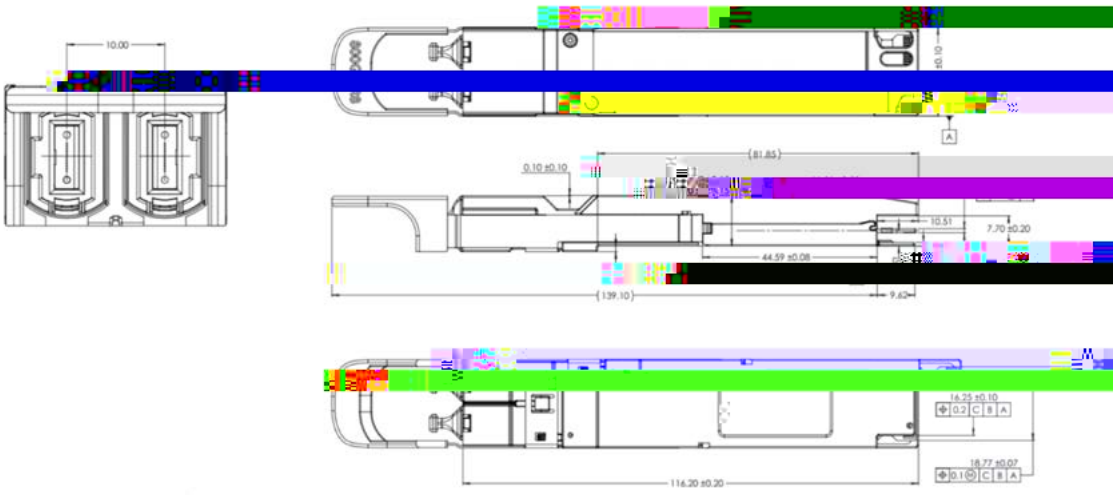
Timing specifications for control inputs and alarm/warning and status indicators are described below. Note that alarm and warning flag thresholds are defined in the respective memory map registers, and the Tx Fault and Rx LOS behavior is outlined in the Fault Behavior section.

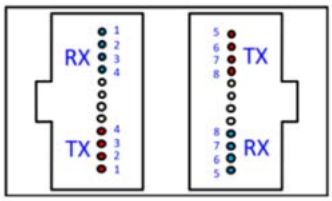
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
MgmtInitDuration			2000	ms	Time from power on (*), hot plug, or rising edge of reset until completion of MgmtInit state
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on ResetL signal to initiate a module reset
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = VOL
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read (**) operation of associated flag until Vout:IntL=VOH. This includes deassert times for Rx LOS, Tx Fault, and other flag bits
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1) and IntL asserted
Rx LOS Deassert Time	toff_losf		3	ms	Time from Rx LOS condition absent to negation of Rx LOS status bit
Tx Disable Assert Time	ton_txdis		100	ms	Time from Tx Disable bit set (value = 1) (***) until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis		400	ms	Time from Tx Disable bit cleared (value = 0) (***) until optical output rises above 90% of nominal
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault condition to the Fault bit set (value = 1) and IntL asserted
Alarm and Warning Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value = 1) and IntL asserted
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value = 1) (***) until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value = 0) (***) until associated IntL operation resumes
Rx Squelch Assert Time	ton_rxsq		15	ms	Time from loss of Rx input signal until squelched output condition is reached
Tx Squelch Assert Time	ton_txsq		400	ms	Time from loss of Tx input signal until squelched output condition is reached
Tx Squelch Deassert Time	toff_txsq		1.5	s	Time from resumption of Tx input signal until normal Tx output condition is reached

For additional information, visit

Mechanical Specifications

The module housing, mechanical features, and electrical connector are compliant with OSFP mechanical specifications. The module optical connector is two standard MPO-12 duplex receptacle (APC) compliant with IEC-61754 and EIA/TIA-604-18.





Label Specification

Ordering Information

JABIL PART NUMBER	DESCRIPTION	PACKAGE	RATE	REACH
OS8CIRMOCxx0PAM	800 Gb/s DR8+ OSFP Optical Transceiver with Dual MPO-12 Optical Connector, 2km Reach	OSFP	850Gb/s	2km
OS8CS3MOCxx0PAM	800 Gb/s DR8 OSFP Optical Transceiver with Dual MPO-12 Optical Connector, 500m Reach	OSFP	850Gb/s	500m

Document Version

VERSION	DATE	NOTES
1.0	11/21/2023	Initial specification version
1.1	7/8/2024	Updated Regulatory and Compliance

Manufacturer’s Address

JABIL CIRCUIT SDN BHD
PMT 772, Persiaran Cassia Selatan 7,
Taman Perindustrian Batu Kawan,
Mukim 13 Batu Kawan
Seberang Perai Selatan
Simpang Empat, Pulau Pinang 14110 Malaysia